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Laung-Terng Wang et al

FILING DATE
February 27, 2002

GROUP
2184

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6,240,377	05/2001	Kai et al	703	24	
	6,199,031	03/2001	Challier et al	703	14	
	6,122,762	09/2000	Kim	714	726	

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FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

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<i>[Signature]</i>	5,488,688	01/1996	Gonzales et al	714	34	
	5,491,793	02/1996	Somasundaram et al	714	45	
	5,544,311	08/1996	Harenberg et al	714	40	
	5,724,505	03/1998	Argade et al	714	45	
	5,828,824	10/1998	Swoboda	714	25	
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FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>[Signature]</i>	J. Ghosh-Dastidar et al, "A Rapid and Scalable Diagnosis Scheme for BIST Environments with a Large Number of Scan Chains," Proc., IEEE VLSI Test Symposium, pp. 79-85, 2000. /COPY ENCLOSED/
	M. Abromovici et al, Digital Systems Testing and Testable Design, Computer Science Press, New York, 1990 /COPY UNAVAILABLE/
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